

Fig1A. Serial termination

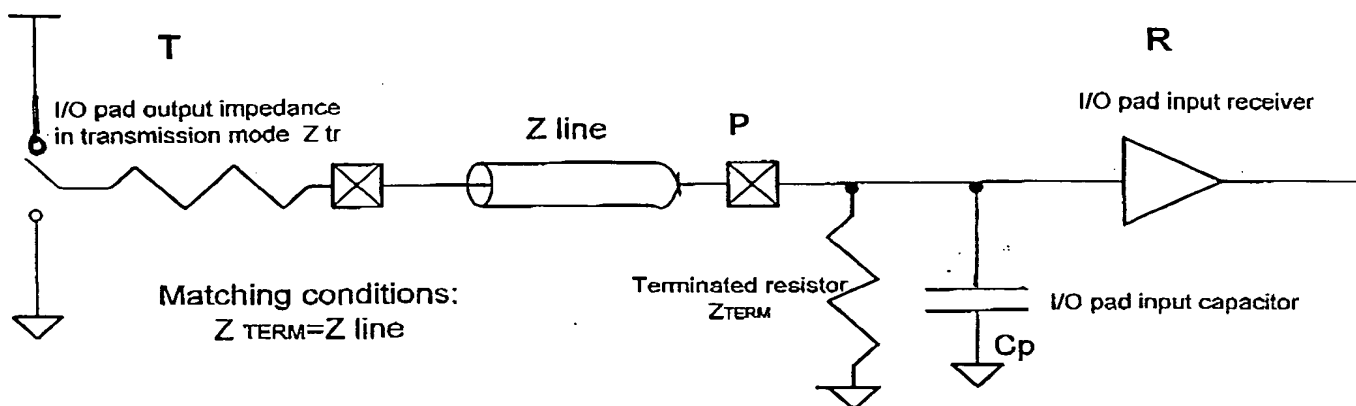


Fig1B. Parallel termination

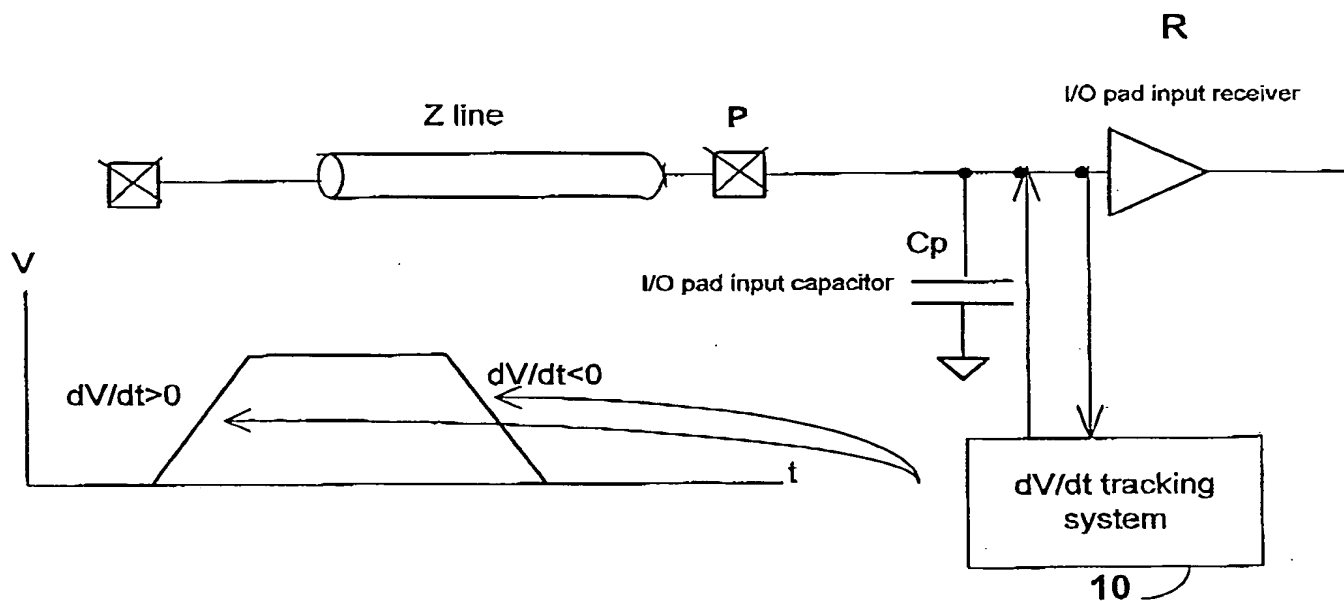


Fig2A.  $dV/dt$  tracking system



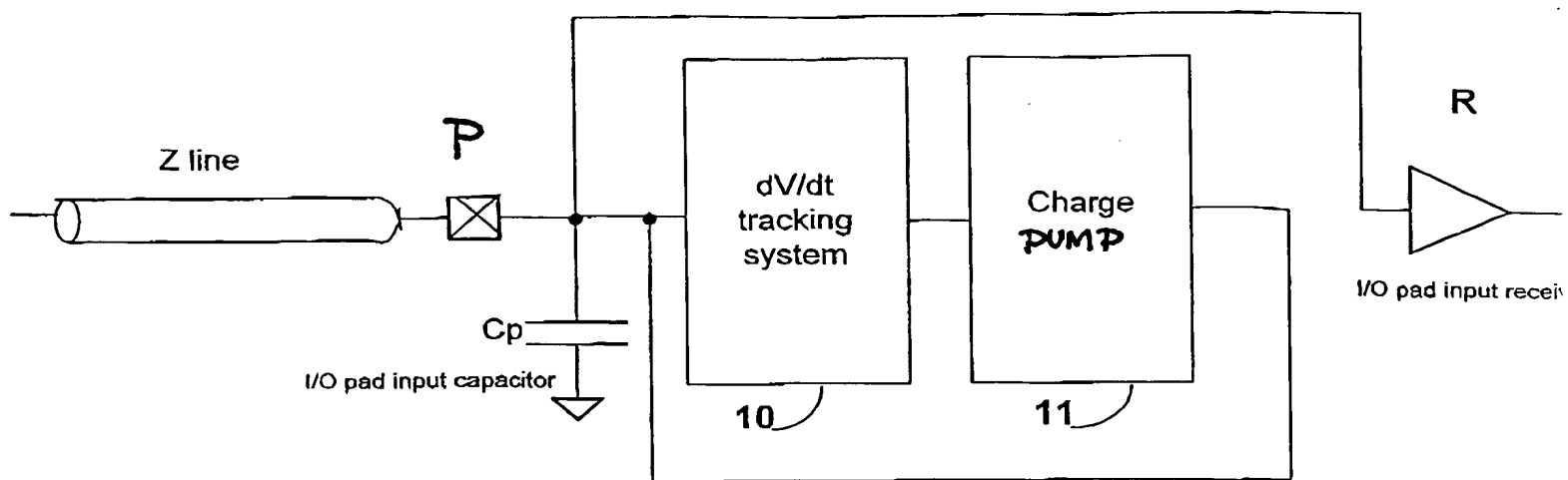


Fig. 2β dV/dt tracking system with charge pump

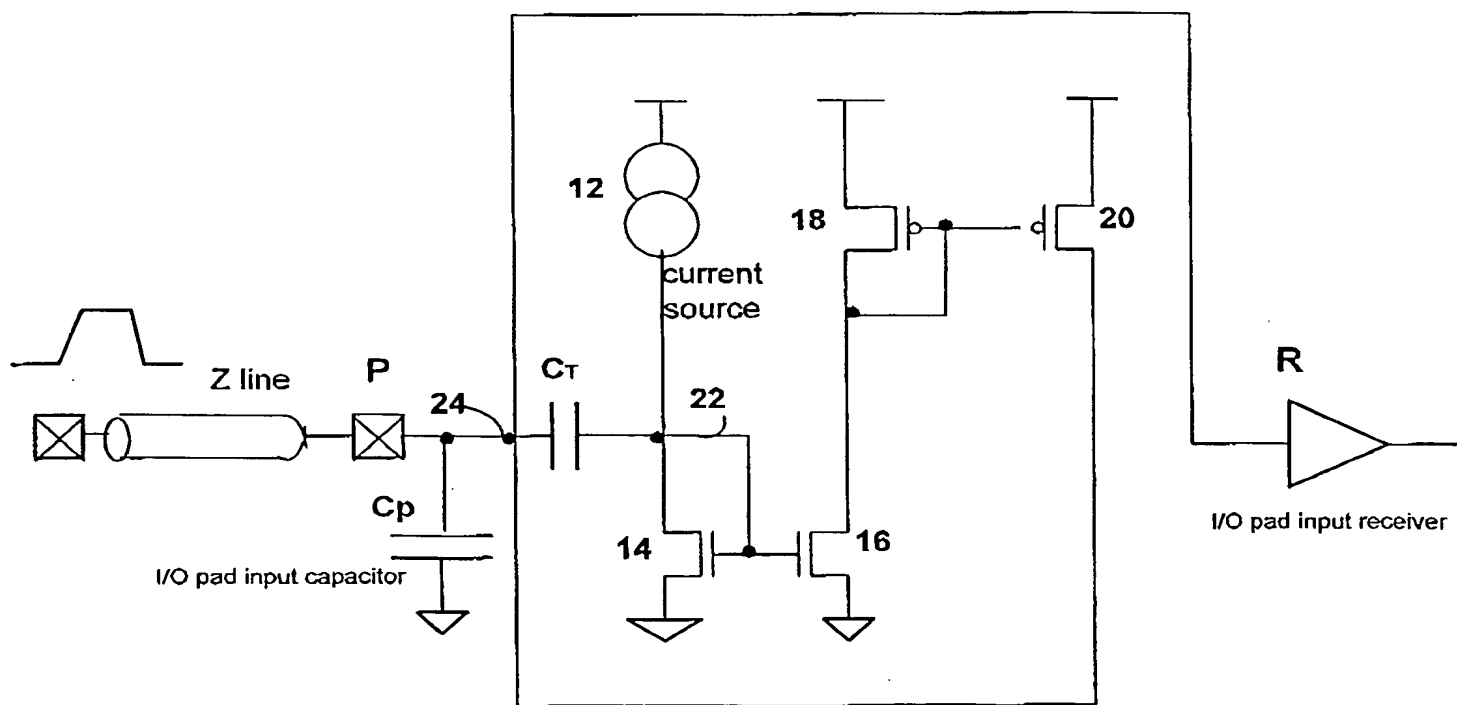
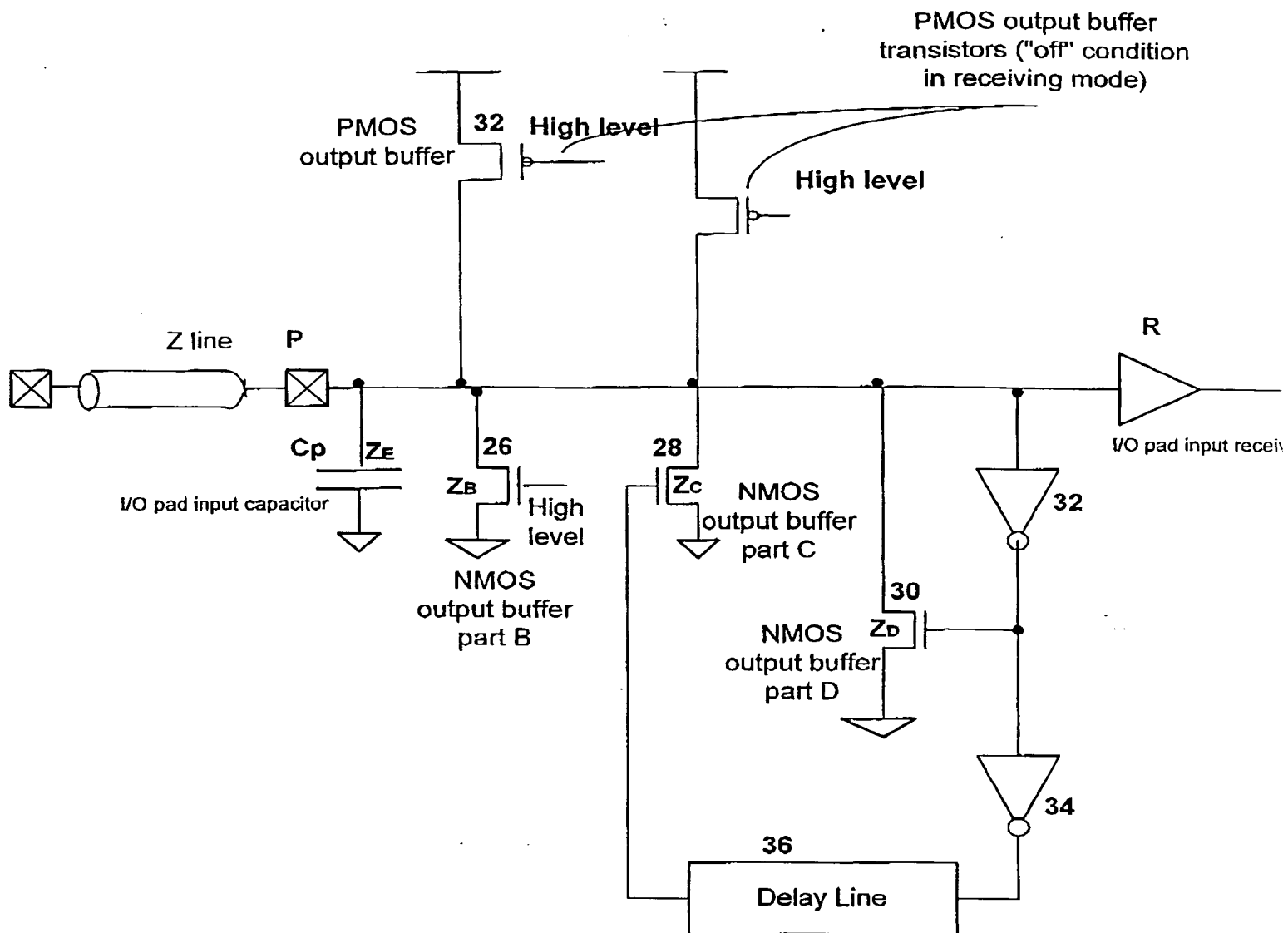


Fig. 2C. dV/dt tracking system with charge pump (more detailed)



$$Z_{\text{input}} = Z_B \parallel [Z_C(\text{or } Z_D, \text{or } Z_E)]$$

if  $|Z_C| = |Z_D| = |Z_E|$ , then an input signal can not change  $Z_{\text{input}}$

Fig. 2D NMOS output buffer parallel termination

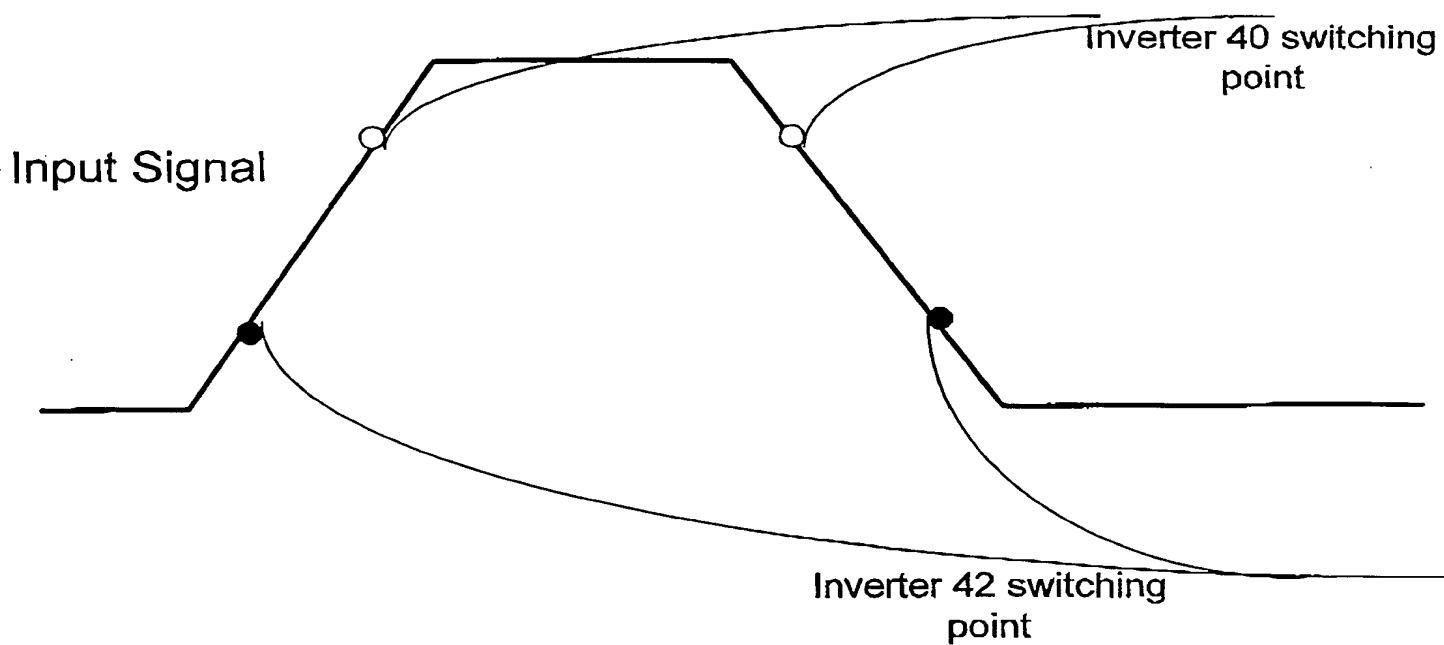
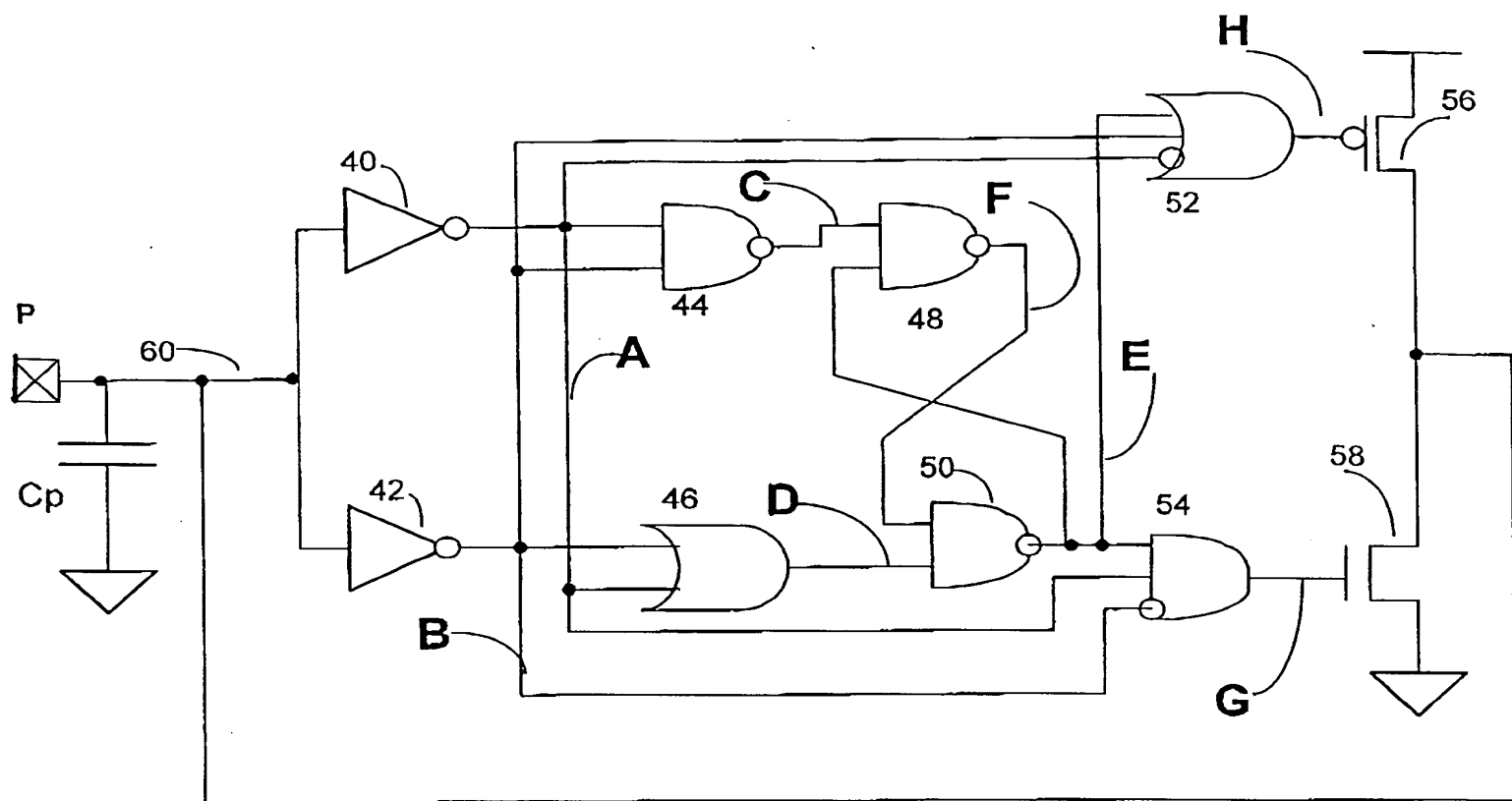


Fig. 3. An input parasitic capacitor charge/discharge circuit

